DOCKET NO. BUR920030106US1

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**In re application of:**
Howard T. Barrett, *et. al.*

**Group Art Unit:** Unknown

**Serial No.:** ~~Not assigned yet~~ 10/605,109

**Examiner:** Unknown

**Filed:** ~~Concurrently herewith~~ 09/09/03

**For: SYSTEM AND METHOD OF AUTOMATICALLY GENERATING KEFT DESIGN DATA**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. 1.56**

Sir:

Under provisions of 37 C.F.R. 1.97 through 1.99 and pursuant to applicant's duty of disclosure under 37 C.F.R. 1.56, applicants respectfully bring the document listed on the attached Form PTO-1449 to the attention of the Examiner in charge of the above-identified application. A copy of the listed document is provided herewith for the convenience of the Examiner.

This citation does not constitute an admission that the cited reference is relevant or material to the claims nor should it be construed as a representation that no other art than that identified exists. It is merely cited as constituting related art of which the applicant is aware.

It is respectfully requested that this document be considered by the Examiner and formally made of record in this application.

Respectfully submitted,

Andrew M. Calderon
Reg. No. 38,093

McGuireWoods LLP
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| SUPPLEMENTAL FORM PTO-1449 (Modified)<br><br>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT<br><br>(Use several sheets if necessary) | ATTY. DOCKET NO.<br>BUR920030106US1<br><br>APPLICANT:<br>Howard T. Barrett, et al.<br><br>FILING DATE: 09/09/03<br>~~Concurrently Herewith~~ | SERIAL NO.<br>~~Unassigned~~ 10/605,109<br><br>GROUP:<br>Unassigned |
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REFERENCE DESIGNATION

**U.S. PATENT DOCUMENTS**

| EXAMINER INITIALS | | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE (IF APPRO.) |
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**FOREIGN PATENT DOCUMENTS**

| | | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | TRANSLATION | |
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**OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)**

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|---|---|---|---|
| | | | K. Ahdoot, et al., "IBM FSD VLSI Chip Design Methodology", Proceedings of Twentieth Design Automation Conference on Design Automation, June 1983, pp. 39-45. |
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| EXAMINER | DATE CONSIDERED |
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.